AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1-5. (canceled)

6. (currently amended) A method for a processor comprising a plurality of datapath elements to process, with reduced power consumption, a sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for a corresponding datapath element of the processor, the method comprising:

fetching an identifier having one bit for each datapath element of the processor, wherein a bit of the identifier corresponding to a first datapath element is set only if ~~a corresponding~~ the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words;

disabling [[an]] a datapath element of the processor, ~~to reduce~~ thereby reducing power consumption by the processor, if the ~~a corresponding~~ bit of the identifier corresponding to that datapath element is set; and, while the datapath element is disabled:

for each control word of the sequence of multiple-instruction control words;

fetching a control word;

the processor executing the control word using the datapath elements that are not disabled.

7. (currently amended) A method in accordance with claim 6, wherein the processor further comprises a plurality of memory banks each associated with [[an]] a datapath element of a processor, the method further comprising:

disabling a memory bank of the plurality of memory banks while the sequence of control words is processed, to reduce power consumption by the processor further, if ~~a corresponding~~ the bit of the identifier corresponding to the associated datapath element is set;

enabling other memory banks of the plurality of memory banks; and

for each control word of the sequence of control words:

storing the control word in the enabled subset of memory banks.

8. (cancelled)

9. (cancelled)

10. (currently amended) A system for processing a compressed sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for [[an]] a datapath element of a processor having a plurality of datapath elements, the system comprising:

a mask latch for storing a compression mask having one bit for each datapath element of the processor, wherein a bit of the compression mask corresponding to a first datapath element is set only if ~~a corresponding~~ the ordered field corresponding to the first datapath element contains a NOP instruction in every multiple-instruction control word of the sequence of control words;

a logic device ~~unit~~ coupled to the mask latch and responsive to the compression mask;

a memory for storing one or more compressed multiple-instruction control words;

a pipelined permute unit, coupled to the logic device ~~unit~~ and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask; and

an instruction register, coupled the pipelined permute unit and operable to present reconstructed multiple-instruction control words to the datapath elements of the processor.

11. (currently amended) A system in accordance with claim 10, wherein the memory comprises a plurality of memory banks coupled to the logic device ~~unit~~, and wherein the logic device ~~unit~~ is operable to disable memory banks in accordance with the compression mask, the memory banks remaining disabled while the sequence of control words is processed, thereby reducing power consumption of the system.

12. (currently amended) A system in accordance with claim 10, further comprising:

a plurality of ~~processing~~ datapath elements coupled to the mask latch and the instruction register and controlled by the reconstructed multiple-instruction control words,

wherein the compression mask is used to disable ~~processing~~ datapath elements of the plurality of ~~processing~~ datapath elements that are unused by all control words of the sequence of multiple-instruction control words, thereby reducing power consumption of the system.

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13. (currently amended) A system in accordance with claim 12, wherein the plurality of ~~processing~~ datapath elements form part of a re-configurable

streaming vector processor, and wherein the sequence of multiple-instruction control words is a sequence of VLIWs describing a dataflow graph.

14. (currently amended) A system for processing, with reduced power consumption, a sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for a datapath element of a processor, the system comprising:

a mask latch for storing a bit mask having one bit for each datapath element, wherein a bit of the bit mask corresponding to a first datapath element is set only if ~~a corresponding~~ the ordered field corresponding to the first datapath element contains a NOP instruction in every multiple-instruction control word of the sequence of control words;

a plurality of memory banks operable to store instructions of a multiple-instruction control word;

a plurality of datapath elements;

a logic device ~~unit~~ coupled to the mask latch, the memory banks and the datapath elements and operable to enable and disable the plurality of memory banks and the plurality of datapath elements, in accordance with the bit mask, before the sequence of control words is processed, thereby reducing power consumption by the system; and

an instruction register, coupled to the memory banks and operable to present instructions the datapath elements.

15. (previously presented) A system in accordance with claim 14, wherein the plurality of datapath elements form part of a re-configurable streaming vector processor, and wherein the sequence of a plurality multiple-instruction control words is a sequence of VLIWs describing a dataflow graph.